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ANALYSIS OF POWER DISSIPATION IN DRAM CELLS DESIGN FOR NANOSCALE MEMORIES

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In this paper power dissipation analysis for DRAM design have been carried out for the Nanoscale memories. Many advanced processors now have on chip instructions and data memory using DRAMs. The major contribution of power dissipation in DRAM is off-state leakage current. Thus, improving the power efficiency of a DRAM cell is critical to the overall system power dissipation. This paper investigates the effectiveness of combination of different DRAM circuit design techniques power dissipation analysis. DRAM cells are designed both with the semantic design technique and layout design technique for the comparison of power dissipation using TANNER CAD Tool. From the results it found that layout technique dissipate less power as compare the semantics technique of DRAM cell.

Keywords: Power Dissipation, Low Power, DRAM, Layout and SPICE Circuit Design.

Introduction

Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital system. The amount of memory required in a particular system depends on the type of application, but number of transistors required for storage function is larger than for logic operations and other application. The ever increasing demand for large storage capacity has driven the fabrication technology and memory development towards more compact design rules and consequently towards higher data storage densities. On-chip memory arrays have become widely used subsystems in VLSI circuits and commercially available single chip read/write memory capacity has reached 1Gb [1, 2]. The semiconductor memory is generally classified according to the type of data storage and data access. Read/write memory or random access memory (RAM) must permit the modification of data bits stored in the memory array, as well as their retrieval demand [3-6]. The stored is volatile; i.e. the store data is lost when the power supply voltage is turned off. In Modern age People in the Electronics industry commonly use the term "memory" to refer to RAM. A computer uses RAM to temporarily hold instructions and data necessary for the CPU (Central Processing Unit) to process tasks. In networking equipment, memory is used to buffer various types of information.

Based on the operation type of individual data storage cells, RAMs are classified into two main categories: dynamic RAM (DRAM) [7-14] and static RAM (SRAM) [2-6]. The SRAM cell consists of latch so the cell data is kept as long as power is turned on and refresh operation is not required. The DRAM cell consists of a capacitor to store binary information and a transistor to access the capacitor. Cell information is degraded mostly due to a junction leakage current at the storage node. Therefore the cell data must be read and rewritten periodically even when memory arrays are not accessed. DRAM is widely used for the main memory in personal and mainframe computers and engineering workstations. SRAM is mainly used for the cache memory in microprocessor, mainframe computers, engineering workstations and memory in handheld devices due to high speed and low power consumption.

In this paper, we have taken two circuits of dynamic random access memory (DRAM). Read and write operation for a single bit storage of both circuits are shown by simulating it on T-spice Layout of both circuits are made and then compare it on the basis of power consumption. With the variation of channel width of transistor, Power consumption variation is also shown.

Dynamic Memory Technologies

As the continuing trend for high density memories favors small memory cell sizes, the dynamic RAM cell with a small structure has become a popular choice, where binary data are stored as a charge in a capacitor and the presence or absence of stored charge determines the value of the stored bit. The data stored in a capacitor cannot retain indefinitely, because the leakage currents eventually remove or modify the stored data. Thus the DRAM cell requires a periodic refreshing of the stored data, so that unwanted modifications due to leakage are prevented before they occur. The usage of a capacitor as a primary storage device generally enables the DRAM cell to be realized in a much smaller silicon area compared to the typical SRAM cell. [1]

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Different DRAM Circuits

The four-transistor cell is shown in Figure 1. Its "write" and "read" operations are similar to those of the SRAM cell. In the "write" operation, a word line is enabled and complementary data are written from a pair of hit lines. Charge is stored at the parasitic and gate capacitances of a node connected with a high voltage hit line. Since no current path is provided to the storage nodes for restoring the charge lost due to leakage, the cell must be- refreshed periodically. In the "read" operation, the voltage of a bit line is discharged to the ground through the transistor where the gate is charged with the high voltage. The read operation is non-destructive since the voltage stored at the node is maintained during the read operation.

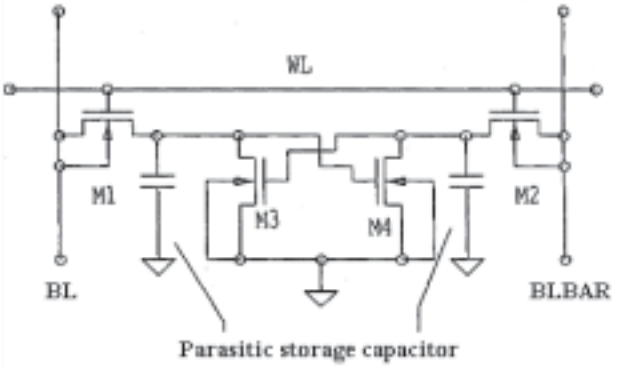

Figure 1: Four-Transistor RAM Cell with Two Storage Nodes

Three-Transistor DRAM Cell

The three transistor cell (Figure 2) utilizes a single transistor (M3) as the storage device (where the transistor is turned on or off depending on the charge stored in its gate capacitance) and one transistor each for the "read" and "write" access switches. During the "write" operation, the write word line is enabled and the voltage of the write bit line is passed on to the gate of storage device through the M1 transistor. During the read operation, the voltage of the read bit line is discharged to the ground through the M2 and M3 transistors when the gate voltage of the storage device is high. The read operation of the three transistor DRAM cell is also non-destructive and relatively fast, but the four lines, i.e., two bit lines and two word lines, with their additional contacts tend to increase the cell area.

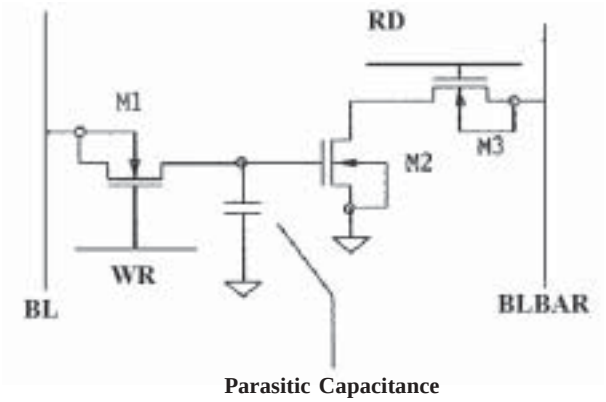

Figure 2: Three Transistor DRAM Cell

Two Transistor DRAM Cell

The 2T DRAM cell (Figure 3) [3] is a simplification of the standard 3T cell popular for on-chip DRAM that gives higher density. During a write, *wbl* (write bit line) is driven with the data, and then raise *wl* (write line) and allow the data to be stored on the *store* node. The charge is held by a combination of gate and diffusion capacitance. Reading a value from the cell is slightly more complicated than the write. The basic operation consists of precharging the read bit line (*rbl*) and allowing the read transistor to turn on by pulling *rl* (read line) low. A logical one will start pulling *rbl* low, while a logical zero will leave the value of *rbl* unchanged. This readout phase is allowed to continue for a preset margin of time, during which time a logical one will drop the voltage on *rbl* to some level V_r. A readout can be completed successfully by comparing V_{rbl} to some reference voltage Vref such that *Vdd > Vref >Vr* via a *differential sense amplifier.* A refresh is accomplished by doing a read onto an internal bus, and then a write from this internal bus. [3]

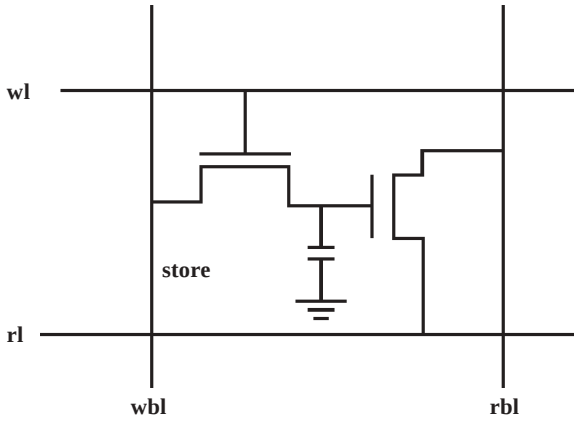

Figure 3: Two Transistor Memory Cell

One complication with a 2T cell is that *Vrbl* will not drop more than two *n*-transistor thresholds below the *Vdd* during the read. The reason can be shown in Figure, where an adjacent bit in the same column has a one stored (thus having *Vdd-V*th stored). If the read bit line should drop more than two thresholds, this transistor will turn on and keep the bit line from falling further; in practice, however, this margin is more than adequate for correct sensing.

Sensing the difference between the read bit line and the reference voltage requires a circuit structure called a

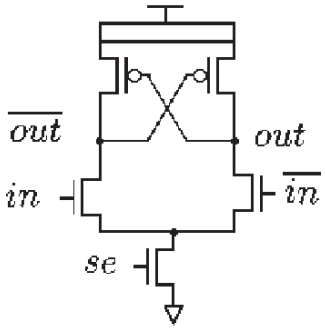

Figure 4: Sense Amplifier

differential sense amplifier, which can convert a difference of several hundred millivolts into a full rail-to-rail transition.

Because most DRAMs are designed with very long bit lines (spanning on the order of hundreds to thousands of rows), the bit line changes that need to be sensed are very small.

One-Transistor DRAM Cell

The one-transistor DRAM cell (Figure 5) [1] has become the industry-standard dynamic RAM cell in high-density DRAM arrays. It has explicit storage capacitor. It means that a separate capacitor must be manufactured for each storage cell, instead of relying on the gate and diffusion capacitances of the transistors for data storage.

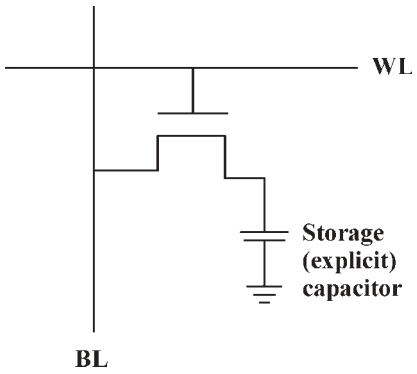

Figure 5: One Transistor DRAM Cell

In the "write" operation, after the word line is enabled, the data are written into the cell through the Ml transistor and stored at the storage capacitor. The read operation is destructive. When the charge stored in the storage cell is shared with the bit line, its charge can he changed significantly (destructed). Also, since the capacitance of the bit line is larger than that of the storage cell by at least about 10 times, only a small voltage difference is produced at the bit line depending on the voltage level (data) of the storage cell. Therefore, an amplifier to sense the signal difference and rewrite the data into the cell (charge restoring operation) is required for the successful "read" operation.

Tanner Output

We have taken here two circuits, i.e. three transistor DRAM and four Transistor DRAM circuit. Read and write operation of these two circuits are simulated in T-spice. Power dissipation is determined and compared for these circuits. We have used nanoscale technology in this project to design the circuit.

Schematic in *S*-Edit

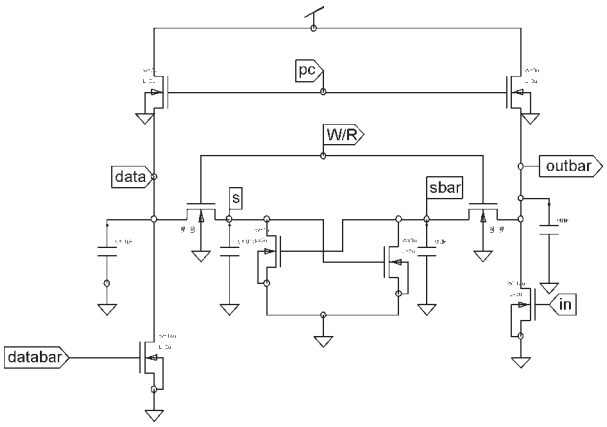

Figure 6: Circuit for 4-Transistor DRAM

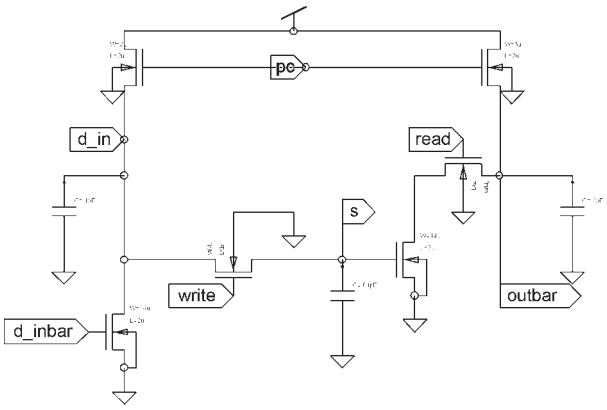

Figure 7: Circuit for 3-Transistor DRAM

Figure 8: Waveform for Read and Write Operation of 4-Transistor DRAM (*S*-Edit)

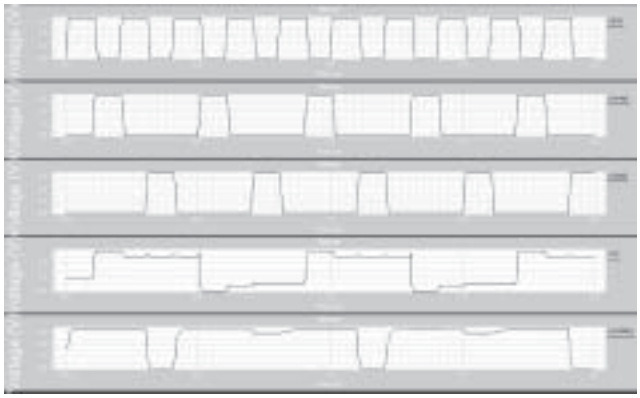

Figure 9: Waveform for Read and Write Operation of 3-Transistor DRAM (*S*-Edit)

RESULT AND CONCLUSION

We have simulated read and write operation of 3 transistor cell and 4 transistor cell. Its power results are as shown below. Layouts are also drawn for these circuits. Simulation of read and write operation of two transistor DRAM cell is successfully done. So we have not included its simulation result.

Power Results for 3-trasistor DRAM designed in project v1 from time 0 to 2e-006

Average power consumed -> 4.044555e-005 watts

Max power 1.657927e-003 at time 1.41e-006

Min power 1.571655e-011 at time 1.04043e-007

Power Results for 4-transistor DRAM designed in project v1 from time 0 to 2e-006

Average power consumed -> 9.180003e-004 watts

Max power 1.830971e-003 at time 5.01162e-007

Min power 5.962186e-011 at time 4e-007

Power Dissipation Result in 4T DRAM

Channel Width of Cell	*Average Power Consumption 4T DRAM*
90 nm	0.923 mW
120 nm	0.9246 mW
180 nm	0.9273mW
0.2 µm	0.929 mW
0.3 µm	0.95 mW

Power Dissipation Result in 3T DRAM

Channel Width of Cell	*Average Power Consumption 3T DRAM*
90 nm	$4.19 * 10^{-5}$ mW
120 nm	$4.655 * 10^{-5}$ mW
180 nm	$5.468 * 10^{-5}$ mW
0.2 µm	$5.917 * 10^{-5}$ mW
0.3 µm	$6.481 * 10^{-5}$ mW

From the above observation it is clear that as the width of transistor used in particular memory cell increases power consumption also increases. We have taken here the optimum width at which the power consumption is minimum as shown in table. It can be also seen from table that four transistor cell has higher dissipation than compare to three transistor cell.

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